Technical Memo

Number: NRF-KAT7-5.0-MEM-008

To : DBE Team

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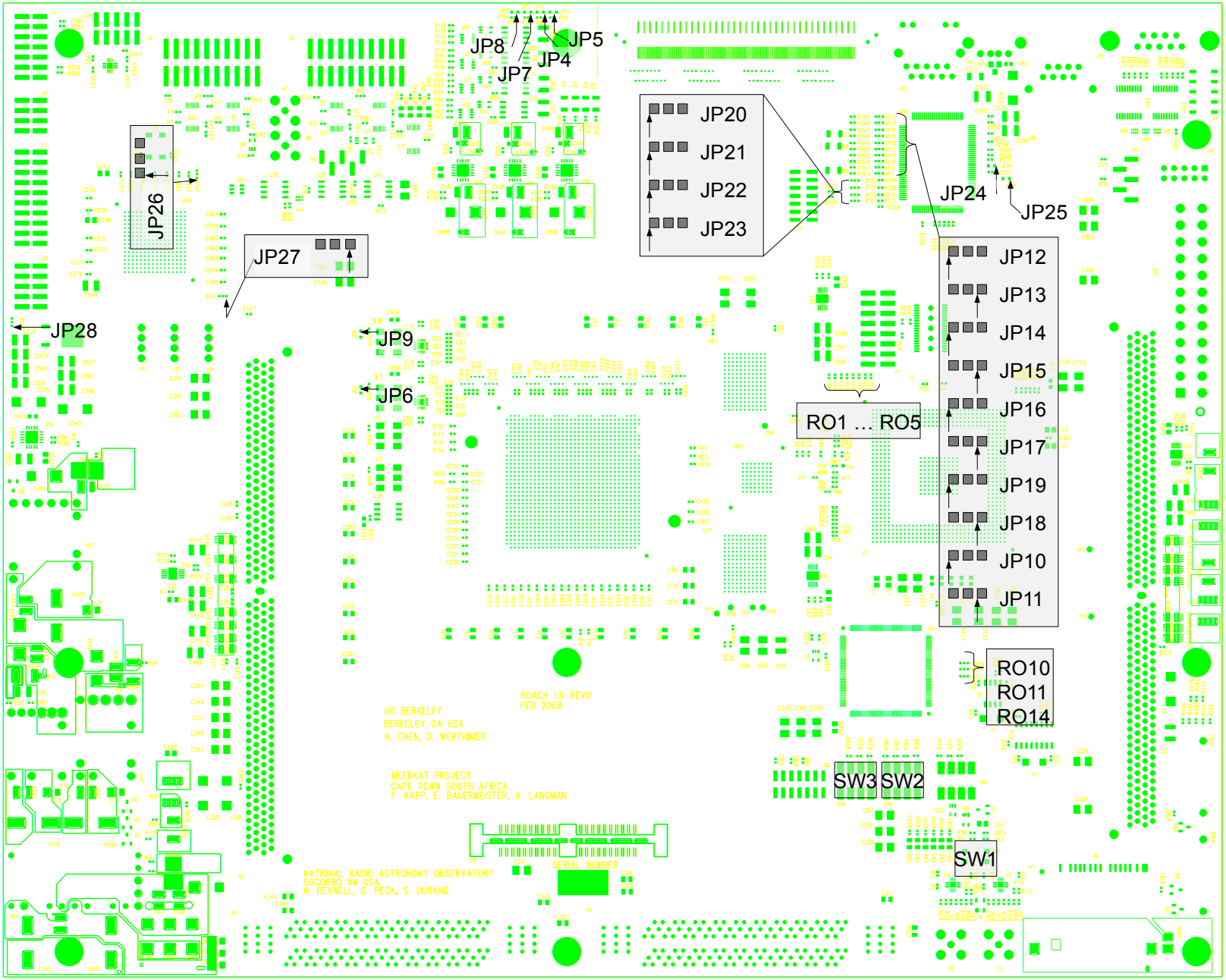
SKA SOUTH AFRICA
SQUARE KILOMETRE ARRAY

Subject: Jumper, DIP and optional resistor settings for ROACH rev 1.02

Location of jumpers, switches and resistors on hardware

The following page shows the layout of a ROACH board. In each case, the arrows indicate the position of pin 1.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ROACH 1.0 REV0
FEB 2008
UC BERKELEY
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Jumper Function summary

The jumper functions are summarized in the tables below.

Two pin jumpers (0805):

Ref Des	Description	Present	Absent
JP4	CN1 Optics Disable	Optics Disabled	**Optics Enabled (default)**
JP5	CN2 Optics Disable	Optics Disabled	**Optics Enabled (default)**
JP6	Ref clock disable: X1 (CN1,CN2)	Disables reference clock output	**Ref clock enabled (Default)**
JP7	CN3 Optics Disable	Optics Disabled	**Optics Enabled (default)**
JP8	CN4 Optics Disable	Optics Disabled	**Optics Enabled (default)**
JP9	Ref clock disable: X4 (CN3,CN4)	Disables reference clock output	**Ref clock enabled (Default)**
JP24	Test: GMCMDIO	Not Allowed	**Test connection for MDIO (Default)**
JP25	Test: GMCMDCLK	Not Allowed	**Test connection for MDCLK (Default)**

Table 1: Two pin jumper settings

Three pin jumpers (0402):

Ref Des	Description	Absent	1-2	2-3
JP10	U58 Duplex LED / PHY Address 0 Strap 1	Both must be connected to allow proper operation	**Address 0 = 0 LED is Active High (Default)**	Address 0 = 1 LED is Active Low
JP11	U58 Duplex LED / PHY Address 0 Strap 0			
JP12	U58 Activity LED / Speed 0 Strap	Both must be connected to allow proper operation	**Speed 0 = 0 LED is Active High (Default)**	Speed 0 = 1 LED is Active Low
JP13	U58 Activity LED / Speed 0 Strap			
JP14	U58 Link10 LED / Speed 1 Strap	Both must be connected to allow proper operation	**Speed 1 = 0 LED is Active High (Default)**	Speed 1 = 1 LED is Active Low
JP15	U58 Link10 LED / Speed 1 Strap			
JP16	U58 Link100 LED / Duplex Strap	Both must be connected to allow proper operation	Half Duplex LED is Active High	**Full Duplex LED is Active Low (Default)**
JP17	U58 Link100 LED / Duplex Strap			
JP18	U58 Link1000 LED / AN Enable Strap	Both must be connected to allow proper operation	Auto Negotiation Disabled LED is Active High	**Auto Negotiation Enabled LED is Active Low (Default)**
JP19	U58 Link1000 LED / AN Enable Strap			
JP20	U58 PHY Address 1 Strap	Not Allowed	**Address 1 = 1 (Default)**	Address 1 = 0
JP21	U58 PHY Address 2 Strap	Not Allowed	**Address 2 = 1 (Default)**	Address 2 = 0
JP22	U58 PHY Address 3 Strap	Not Allowed	**Address 3 = 1 (Default)**	Address 3 = 0
JP23	U58 PHY Address 4 Strap	Not Allowed	**(MSB) Address 4 = 1 (Default)**	Address 4 = 0
JP26	ROACH Monitor U60 VCC_PLL_A	Not Allowed	PLL A powered down	**PLL A power on (Default)**
JP27	ROACH Monitor U60 VCC_PLL_B	Not Allowed	PLL B powered down	**PLL B power on (Default)**
JP28	ROACH Monitor U60 Programming Charge Pump Enable	Not Allowed	Charge Pump Disabled	**Charge Pump Enabled (Default)**

Table 2: Three pin jumper settings

Jumper Description

JP1, JP2

No longer in existence.

JP4, JP5, JP7, JP8

Optics module disable. The CX4 output connectors contain special connections on the designated ground pins in order to power CX4 to optical conversion modules like the Fujitsu FPD-010R008-0E. These modules can be disabled by pulling the signal on the ODIS input high. JP4, when present will disable the optical module. The default is to have the jumper not populated.

JP4 configures CN1, JP5 configures CN2, JP7 configures CN3, JP8 configures CN4.

JP6, JP9

GTP Reference clock output disable. Disables the output of the clock generator X1 and clock distribution device U8 if present. Potential power savings for applications not requiring all GTP's. JP6 affects locations CN1 and CN2. JP9 affects locations CN3 and CN4.

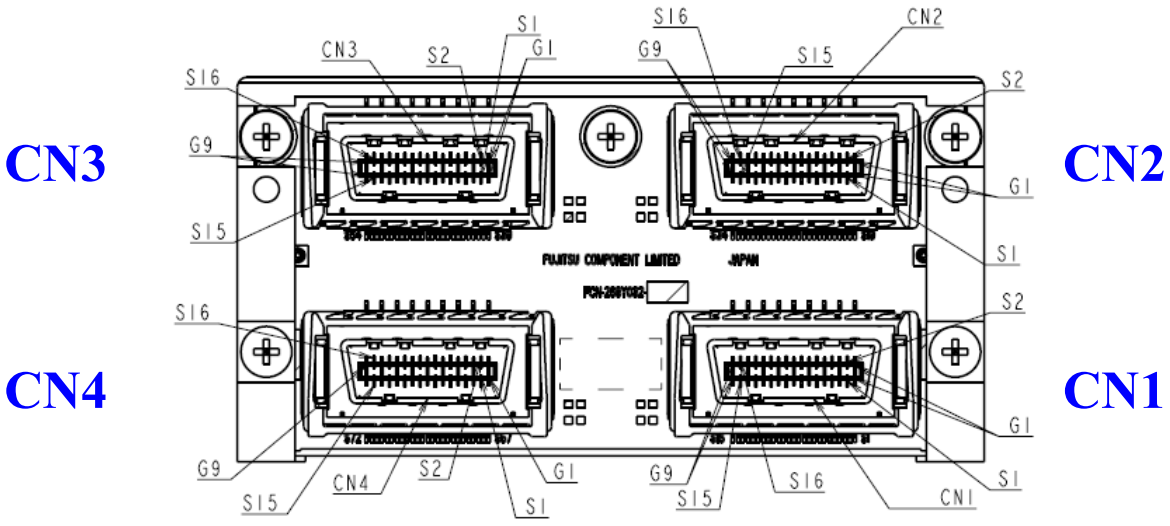


Figure 1: Connector location for optical module jumper controls

JP10 and JP11

These two jumpers operate in tandem and must always be connected to the same pin pairs of the two locations. They control the operation of the Ethernet PHY (U58) Duplex LED and act as the strapping input for PHY Address 0 Strap 1. This is the LSB of the 5 bit PHY address. The default location is both jumpers present between pins 2 and 3, setting the address to 1 and the LED to active low operation. The remainder of the address inputs are controlled by JP20-23. See the National DP83865 data sheet, pages 10 and 67 for more information.

JP12 and JP13; JP14 and JP15

These jumper pairs operate in tandem and must always be connected to the same pin pairs of the two locations. JP12 and JP13 control the operation of the Ethernet PHY (U58) Activity LED and act as the strapping input for Speed 0. JP14 and JP15 control the operation of the Ethernet PHY (U58) Link10 LED and act as the strapping input for Speed 1. The default location is for all four jumpers present between pins 1 and 2, setting the speed to 00 and the LED's to active high operation. This, together with the auto-negotiation strapping input places the device into a mode where 10BASE-T, 100BASE-T and 1000BASE-T is enabled through auto-negotiation.

JP16 and JP17

These jumpers operate in tandem and must always be connected to the same pin pairs of the two locations. They control the operation of the Ethernet PHY (U58) Link100 LED and act as the strapping input for duplex. The default location is for both jumpers present between pins 2 and 3, enabling full duplex mode and setting the LED's to active low operation.

JP18 and JP19

These jumpers operate in tandem and must always be connected to the same pin pairs of the two locations. They control the operation of the Ethernet PHY (U58) Link1000 LED and act as the strapping input for Auto-Negotiation (AN). The default location is for both jumpers present between pins 2 and 3, enabling auto negotiation and setting the LED's to active low operation.

JP20, JP21, JP22 and JP23

These jumpers control the Ethernet PHY (U58) strapping inputs for PHY Address 1, 2, 3, and 4 respectively. These are the MSB's of the 5 bit PHY address, with Address 4 being the MSB. The default location is both jumpers present between pins 1 and 2, setting the address to 0 and the LED to active low operation. Address0 is controlled by JP10-11. See the National DP83865 data sheet, pages 10 and 67 for more information.

JP24

This is not strictly a jumper, but a test point with ground for the GMCMDIO signal of U58. Pin 1 is ground. Do not place a jumper in this location.

JP25

This is not strictly a jumper, but a test point with ground for the GMCMDCLK signal of U58. Pin 1 is ground. Do not place a jumper in this location.

JP26

Roach monitor (U60) PLL A Enable. Power to the phase locked loop of U60. Default is jumper present between pins 2 and 3, enabling the PLL. If the PLL is unused, this jumper can be changed to position 1-2 to reduce power consumption.

JP27

Roach monitor (U60) PLL B Enable. Power to the phase locked loop of U60. Default is jumper present between pins 2 and 3, enabling the PLL. If the PLL is unused, this jumper can be changed to position 1-2 to reduce power consumption.

JP28

Roach monitor (U60) charge pump enable. Enables or disables the programming voltage of U60. Default is jumper present between pins 2 and 3, enabling the programming voltage generation. If the device will not be or is required not to be reprogrammed, this jumper can be changed to position 1-2 to reduce power consumption.

Optional Resistors

By default, none of these resistors should be populated.

RO1

Optional pull-down on PowerPC IRQ9. This pin is used in ROACH as GPIO to interface to the TDO JTAG pin of the Virtex 5.

RO2

Optional pull-down on PowerPC IRQ8. This pin is used in ROACH as GPIO to interface to the TMS JTAG pin of the Virtex 5.

RO3

Optional pull-down on PowerPC IRQ7. This pin is used in ROACH as GPIO to interface to the TCK JTAG pin of the Virtex 5.

RO4

Optional pull-down on PowerPC IRQ6. This pin is used in ROACH as GPIO to interface to the TDI JTAG pin of the Virtex 5.

RO5

Optional pull-down on PowerPC IRQ4. This pin is used in ROACH as GPIO44.

RO10

Optional pull-up (2-3) or pull-down (1-2) on BOOT_CFG0. This is not required as BOOT_CFG0 is driven from CPLD. Pin 3 is 3v3 rail. Pin 1 is ground.

RO11

Optional pull-up (1-2) or pull-down (2-3) on BOOT_CFG1. This is not required as BOOT_CFG1 is driven from CPLD. Note: mounted reverse to RO10 and RO14. Pin 1 is 3v3 rail, but because it's reverse mounted, all ground and 3v3 rails align.

RO14

Optional pull-up (2-3) or pull-down (1-2) on BOOT_CFG2. This is not required as BOOT_CFG2 is driven from CPLD. Pin 1 is ground.

Control Signals

RESET_POR#

Controlled by U31 on power up and when the reset button is pressed. Connected to CPLD (U54, pin 143) and PowerPC (U1, SYSRESET#, pin AD31). Causes a PowerPC reset. This in turn will cause the FPGA to be re-configured.

SEL_SYSCLK

Selects the system clock for the PowerPC. Driven by the CPLD (U54, pin 136) it selects the output clock on U9.

GETH0_RST#

Reset to Ethernet PHY (U58).

PPC_DDR2_RESET_N

Reset to PowerPC DDR2 module.

DIP Switches

SW1

PowerPC reset switch.

SW2

Also known as the *user* DIP switch. Default: all off. These switches all have soft functions (reprogrammable by CPLD, U54). With default programming, the switches perform the following functions:

1. Not yet assigned.
2. Not yet assigned.
3. Not yet assigned.
4. Disable write access to EEPROM.

SW3

Also known as the *config* DIP switch. Default: all off. These switches all have soft functions, reprogrammable by CPLD, U54. With default programming, this switch controls the booting of the PPC.

There is a flag in sysconfig on the Actel Fusion to select if ROACH's PPC should pull its configuration out of EEPROM via I2C ("Bootstrap Option H"), or if it should fall-back to hard-coded, pre-defined configurations. By default, ROACHs come with this flag set. The EEPROM is set to boot with a 500MHz PPC core clock and 83MHz peripheral bus. If the flag is not set in the Actel and all switches are off, it will select "Bootstrap Option C", 533MHz CPU and 66MHz bus.

Alternatively, boot modes can be forced (irrespective of the flag in the Actel) by turning on the switches as follows:

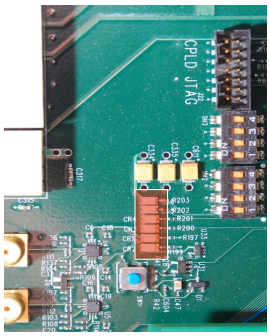
1. Force PPC Fast (peripheral bus at 66MHz, CPU at 533MHz) ("Bootstrap Option C").
2. Force PPC Slow (peripheral bus at 66MHz, CPU at 333MHz) ("Bootstrap Option B").
3. Not yet assigned.
4. Not yet assigned.

Bit 2 has higher priority than bit 1, so if both are "on", " Bootstrap Option B" is selected. The selected bootstrap option can be observed when uBoot boots. It is displayed along with the serial number, memory configuration and other board settings.

See the section "8. Bootstrap Controller" in the PPC440 Users Manual for further information on the various bootstrap options.

Power rail status LEDs

Note that the positions of CR1 and CR2 are flipped in relation to CR3, 4, 5 and 6.



CR1 (Green)

Power present 5V (resistor pullup to 5V rail).

CR2 (Green)

Power good 3v3 (logic signal from PSU).

CPLD LEDs

CR3 (Green)

User LEDs configurable from PPC. Memory mapped to PPC over peripheral bus.

CR4 (Green)

User LEDs configurable from PPC. Memory mapped to PPC over peripheral bus.

CR5 (Red)

Status LED. Constant on: FPGA done programming. Flashing: PPC system error.

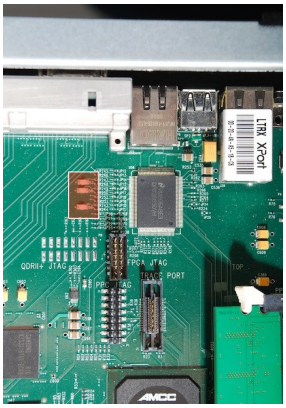
CR6 (Red)

Flash busy (read or write).

1GbE PHY LEDs

Default functions change depending on jumper and software settings.

By default, ROACH is configured for:



D6 (Red)

Duplex status: On = Full duplex, off=Half duplex or no link.

D7 (Red)

10Mbps link: On = 10Mbps link active.

D8 (Red)

100Mbps link: On = 100Mbps link active.

1GbE “RJ45” socket

Contains 2 LEDs. The green one indicates 1000Mbps link is established.

The amber one flashes with link activity.

Additional Notes

There is an onboard connector for the PPC's second serial port (J14) located directly behind the first serial port.

Pinout as follows:
1 = NC
2 = RX
3 = TX
4 = 5V supply
5 = GND
6 = RTS
7 = CTS
9 = NC
10 = NC