<table>
<thead>
<tr>
<th>Jumper pins</th>
<th>Pitch</th>
<th>size</th>
<th>Vendor</th>
<th>Part</th>
<th>Signal to use</th>
<th>signal name</th>
<th>shunt installed</th>
<th>shunt gone</th>
<th>holes</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 0</td>
<td>0.1&quot; J7, 16, 12</td>
<td>GPIO2_0</td>
<td>Lsbit 0 of MAC and IP addr, s0</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 0</td>
<td>0.1&quot; J7, 16, 12</td>
<td>GPIO1_6, 4, 2, 0</td>
<td>Msbit walsh sel: input 1</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 0</td>
<td>0.1&quot; J7, 16, 12</td>
<td>GPIO2_11</td>
<td>Lsbit 8 of MAC &amp; IP addr, a3</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 0</td>
<td>0.1&quot; J7, 16, 12</td>
<td>GPIO1_13</td>
<td>midbit walsh sel: input 3</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 0</td>
<td>0.1&quot; J7, 16, 12</td>
<td>GPIO1_12</td>
<td>Lsbit walsh sel: input 3</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 15</td>
<td>0.1&quot; J5, 14, 12</td>
<td>GPIO2_8</td>
<td>Lsbit 8 of MAC &amp; IP addr, a0</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 15</td>
<td>0.1&quot; J5, 14, 12</td>
<td>GPIO1_4</td>
<td>Lsbit walsh sel: input 1</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 15</td>
<td>0.1&quot; J5, 14, 12</td>
<td>GPIO1_10</td>
<td>Msbit walsh sel: input 2</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 15</td>
<td>0.1&quot; J5, 14, 12</td>
<td>GPIO1_8</td>
<td>Lsbit walsh sel: input 2</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 15</td>
<td>0.1&quot; J5, 14, 12</td>
<td>GPIO1_9</td>
<td>midbit walsh sel: input 2</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 15</td>
<td>0.1&quot; J5, 14, 12</td>
<td>GPIO2_12</td>
<td>Lsbit 12 of MAC &amp; IP addr, r0</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 15</td>
<td>0.1&quot; J5, 14, 12</td>
<td>GPIO1_16</td>
<td>Lsbit walsh sel: input 3</td>
<td>pin connected</td>
<td>-</td>
</tr>
<tr>
<td>J2 J7 J12</td>
<td>0.1&quot;</td>
<td>x 2</td>
<td>Samtec</td>
<td>559, 102, 20, 15</td>
<td>0.1&quot; J5, 14, 12</td>
<td>GPIO2_0</td>
<td>Lsbit 0 of MAC and IP addr, s7</td>
<td>pin connected</td>
<td>-</td>
</tr>
</tbody>
</table>

Notes:
- All shunts are black unless otherwise designated.
- Gray: shunts for 0.1" board; Blue: shunts for 0.15" board.
- The examples are based on the assumption that all J8 pins are defined for mode/configuration jumpers.
J10 1,2 0.1" x 0.1" 2 x 8 SNT_100_BK_G DIPSW_SIGS<0> DIPSW_SIGS<0> is shorted to GND. DIPSW_SIGS<0> is pulled to 2.5V

J10 3,4 SNT_100_BK_G DIPSW_SIGS<1> DIPSW_SIGS<1> is shorted to GND. DIPSW_SIGS<1> is pulled to 2.5V

J10 5,6 SNT_100_BK_G DIPSW_SIGS<2> DIPSW_SIGS<2> is shorted to GND. DIPSW_SIGS<2> is pulled to 2.5V

J10 7,8 SNT_100_BK_G DIPSW_SIGS<3> DIPSW_SIGS<3> is shorted to GND. DIPSW_SIGS<3> is pulled to 2.5V

J10 9,10 SNT_100_BK_G DIPSW_SIGS<4> DIPSW_SIGS<4> is shorted to GND. DIPSW_SIGS<4> is pulled to 2.5V

J10 11,12 SNT_100_BK_G DIPSW_SIGS<5> DIPSW_SIGS<5> is shorted to GND. DIPSW_SIGS<5> is pulled to 2.5V

J10 13,14 SNT_100_BK_G DIPSW_SIGS<6> DIPSW_SIGS<6> is shorted to GND. DIPSW_SIGS<6> is pulled to 2.5V

J10 15,16 SNT_100_BK_G DIPSW_SIGS<7> DIPSW_SIGS<7> is shorted to GND. DIPSW_SIGS<7> is pulled to 2.5V

J11 1,2 0.1" 1 x 3 SIP 1x3 SNT_100_BK_G MGT_BOTTOM_CLK_M pin 2 must be J11 and J12 shunts must be in same position!

J11 2,3 0.1" 1 x 3 SIP 1x3 SNT_100_BK_G MGT_BOTTOM_CLK_P tied to pin 3 (or pin 1 shown above)

J12 1,2 0.1" 1 x 3 SIP 1x3 SNT_100_BK_G MGT_BOTTOM_CLK_M pin 2 must be J11 and J12 shunts must be in same position!

J12 2,3 0.1" 1 x 3 SIP 1x3 SNT_100_BK_G MGT_BOTTOM_CLK_P tied to pin 3 (or pin 1 shown above)

J13 1,2 0.1" 1 x 3 SIP 1x3 SNT_100_BK_G MGT_TOP_CLK_M pin 2 must be J13 and J14 shunts must be in same position!

J13 2,3 0.1" 1 x 3 SIP 1x3 SNT_100_BK_G MGT_TOP_CLK_P tied to pin 3 (or pin 1 shown above)

J14 1,2 0.1" 1 x 3 SIP 1x3 SNT_100_BK_G MGT_TOP_CLK_M pin 2 must be J13 and J14 shunts must be in same position!

J14 2,3 0.1" 1 x 3 SIP 1x3 SNT_100_BK_G MGT_TOP_CLK_P tied to pin 3 (or pin 1 shown above)

J15 1,2 0.1" x 0.1" 2 x 3 SIP 2x3 SNT_100_BK_G FPGA_CFGMODE0; U1.AF26 M0 = 0 M0 = 1 See table below

J15 3,4 SNT_100_BK_G FPGA_CFGMODE1; U1.AE26 M1 = 0 M1 = 1 See table below

J15 5,6 SNT_100_BK_G FPGA_CFGMODE2; U1.AE25 M2 = 0 M2 = 1 See table below

J16 1,2 0.1" x 0.1" 2 x 3 SIP 2x3 SNT_100_BK_G REV_SEL_MODE0: U2-25 design revision set by REV_SEL_MODE1:2 bits Internal revision select control bits

J16 3,4 SNT_100_BK_G REV_SEL_MODE1:2-25 when enabled by REV_SEL_MODE stint installed, otherwise ignored

J16 5,6 SNT_100_BK_G REV_SEL_MODE0:U2-27 when enabled by REV_SEL_MODE stint installed, otherwise ignored

XTAL2 125.00 Mhz; note many boards do NOT have 125MHz XTALs

XTAL3 156.25 Mhz; many boards only have 156.25 Mhz XTALs

XTAL2 125.00 Mhz; installed and thus this mode may be nonfunctional. pin 3s are labeled

XTAL3 156.25 Mhz; many boards only have 156.25 Mhz XTALs

XTAL2 125.00 Mhz; installed and thus this mode may be nonfunctional. pin 3s are labeled

XTAL3 156.25 Mhz; many boards only have 156.25 Mhz XTALs

XTAL2 125.00 Mhz; note many boards do NOT have 125MHz XTALs

XTAL3 156.25 Mhz; note many boards do NOT have 125MHz XTALs

M2:M1:M0 = 0b110 = Slave SelectMap Mode. Virtex II Pro FPGA is programmed 8bits at a time from memory mapped writes over the cPCI bus. This is the default.

M2:M1:M0 = 0b111 = Slave Serial Mode. Virtex II Pro FPGA is programmed 1bit at a time from memory mapped writes over the cPCI bus (saves 7 pins over Slave Select Map).

M2:M1:M0 = 0b101 = JTAG (boundary scan) programming; reccommended for programming the PROM and is specified in the official iBob initial test procedure

M2:M1:M0 = 0b011 = Master SelectMAP mode. This is the default. iBPU is the source of cCLK,DONE and INIT_B(to PROM's RESET_/OE)

M2:M1:M0 = 0b010 = Master SelectMAP mode. This is the default. iBPU is the source of cCLK,DONE and INIT_B(to PROM's RESET_/OE)

M2:M1:M0 = 0b001 = Slave Select MAP Mode. Virtex II Pro FPGA is programmed 8bits at a time from memory mapped writes over the cPCI bus. This is the default.

M2:M1:M0 = 0b111 = Slave Serial Mode. Virtex II Pro FPGA is programmed 1bit at a time from memory mapped writes over the cPCI bus (saves 7 pins over Slave Select Map).

M2:M1:M0 = 0b101 = JTAG (boundary scan) programming; reccommended for programming the PROM and is specified in the official iBob initial test procedure

M2:M1:M0 = 0b011 = Master SelectMAP mode. This is the default. iBPU is the source of cCLK,DONE and INIT_B(to PROM's RESET_/OE)
**Jumper pins** | **Pitch** | **size** | **PCB conn.** | **Connector** | **Connector** | **signal name** | **Mating connector** | **notes**
---|---|---|---|---|---|---|---|---
J6 | 1 to 40 | 0.1 x 0.1" | 2 x 20 | DIP 2 x 20 | XP900_0 | 0, 19 | GPIO0; 0, 19 | Closest to the FPGA, pin 1 marked with "o"; all even pins=GND
J6 | 1.5, 9, 13, 17, 21, 25, 29 | 0.1 x 0.1" | 2 x 20 | DIP 2 x 20 | XP900_0 | 0, 19 | GPIO0; 0, 2, 4, 6, 8, 10, 12, 14 | External sync-out signals for syncing standalone iBobs when no external sync signal is available.
J7 | 1 to 40 | 0.1 x 0.1" | 2 x 20 | DIP 2 x 20 | XP901_0 | 0, 19 | GPIO1; 0, 19 | Just closer to PCB edge than J6, pin 1 marked with "o"; all even pins=GND
J8 | 1 to 40 | 0.1 x 0.1" | 2 x 20 | DIP 2 x 20 | XP902_0 | 0, 19 | GPIO2; 0, 19 | Closest to PCB edge, pin 1 marked with "o"; all even pins=GND
J9 | 1 to 40 | 0.1 x 0.1" | 2 x 20 | DIP 2 x 20 | XP903_0 | 0, 19 | GPIO3; 0, 19 | Just farther from PCB edge than J8, pin 1 marked with "o"; all even pins=GND
J11 | 1 to 2 | 0.1" | 1 x 2 | SIP 1 x 2 | Samtec | TS102_26_L1_5 | +5VDC for fan | Molex | 48-50-0114 | Two (2) KK-Series female 2.54 AWG crimp terminals
J11 | 1 to 2 | 0.1" | 1 x 2 | SIP 1 x 2 | Samtec | TS102_26_L1_5 | +5VDC for fan | Molex | 48-30-0107 | KK series 3-pin housing
J17 | 1 to 9 | 0.1" | 1 x 9 | SIP 1 x 9 | Samtec | TS109_14_L1_5 | JTAG | Molex | 12-30-0108 | VCC/2, 5, GND, NC, JTAG, TCK, NC, JTAG, TDI, JTAG, TDO, JTAG, TMS
J18 | 1 to 5 | 0.1" | 1 x 5 | SIP 1 x 5 | Samtec | TS105_12_L1_5 | JTAG | Molex | 48-30-0107 | VCC/2, 5, GND, NC, JTAG, TCK, NC, JTAG, TDI, JTAG, TDO, JTAG, TMS
J19 | 1 to 2 | 0.072" | 1 x 2 | SIP 1 x 2 | Molex | 48620-2212 | VCC5 | Molex | 42815-0011 | Two (2) 12 AWG Mini-Fit Jr. power cable crimp terminals
J19 | 1 to 2 | 0.072" | 1 x 2 | SIP 1 x 2 | Molex | 48620-2212 | VCC5 | Molex | 42816-0212 | 2-pos Mini-Fit Jr. power cable housing
J20 | 1 to 25 | INFIBAND 4X | Molex | 91804-0410 | Top infiband link 0 | Molex | 91804-0410 | Top infiband link 0 | Also has 6 mounting pins; this connector gets screwed to the PCB
J21 | 1 to 26 | INFIBAND 4X | Molex | 91804-0410 | Bottom infiband link 0 | Molex | 91804-0410 | Bottom infiband link 0 | Also has 6 mounting pins; this connector gets screwed to the PCB
J22 | 1 to 144 | 40-PAIR LVDS Z-DOK+ Host | Tyco | 8387550-5 | ADC0 diff. inputs | Tyco | 8387550-5 | ADC0 diff. inputs | U22 is closer to the 100 Mbit connector
J23 | 1 to 144 | 40-PAIR LVDS Z-DOK+ Host | Tyco | 8387550-5 | ADC1 diff. inputs | Tyco | 8387550-5 | ADC1 diff. inputs | U23 is closer to the VDC input power connector
J24 | 1 to 80 | MDR | Molex | N10280-50E2VC | LVDS_Detect, MP[0..39] | Molex | N10280-50E2VC | LVDS_Detect, MP[0..39] |
J115 | 1 to 12 | 0.072" | 1 x 2 | SIP 1 x 2 | Pulse | 300110310 | P117, TPO, TPL, LAN, LED, CAT 5e, cable | Pulse | 300110310 | P117, TPO, TPL, LAN, LED, CAT 5e, cable
J24 | 1 to 80 | MDR | Molex | N10280-50E2VC | LVDS_Detect, MP[0..39] | Molex | N10280-50E2VC | LVDS_Detect, MP[0..39] | Only available on v1 rev2 and v1 rev3 boards
J24 | 1 to 80 | MDR | Molex | N10280-50E2VC | LVDS_Detect, MP[0..39] | Molex | N10280-50E2VC | LVDS_Detect, MP[0..39] | Some of the v1 rev2 iBobs have faults that cause bitstream failures

**Jumper Page as well: part of J7 is used for mode/config jumpers**

**Jumper Page as well: part of J8 is used for mode/config jumpers**

**Jumper Page as well: part of J9 is used for mode/config jumpers**

**BWRC iBob jumper settings**

These aren't jumpers exactly but they are connectors and have Jxx reference designators.

**LVTTL**

- GPIO0_0, 2, 4, 6, 8, 10, 12, 14: External sync-out signals for syncing standalone iBobs when no external sync signal is available.
- GPIO3_16: Walsh output for input 0; for monitoring or driving level shifters/mixers etc
- GPIO3_17: Walsh output for input 1; for monitoring or driving level shifters/mixers etc
- GPIO3_18: Walsh output for input 2; for monitoring or driving level shifters/mixers etc
- GPIO3_19: Walsh output for input 3; for monitoring or driving level shifters/mixers etc

**J115 Jumper Pins Test**

These are I/O pins used for testing purposes.

- J115 pin 1: 5VDC power supply
- J115 pin 2: Ground
- J115 pin 3: Test signal A
- J115 pin 4: Test signal B

**J115 Jumper Pins Test**

These are I/O pins used for testing purposes.

- J115 pin 1: 5VDC power supply
- J115 pin 2: Ground
- J115 pin 3: Test signal A
- J115 pin 4: Test signal B