PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND

PLACE AT MODULE VDDSPD PIN

PLACE AT MODULE VREF PIN

PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND
Place components close to CPU

REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF – INCLUDED ON ROACH_PCIE_DOR2
REMOVED 3V3 GENERATION

REMOVED +12V GENERATION
REMOVED -12V GENERATION

REMOVED +1V GENERATION
REMOVED +2V5 GENERATION

Please wire cap at each corner of the PCB.
PCI BUS NOT IMPLEMENTED
The Tx and the RX side trace length should be equal to each other. Place components as close to PHY all the time.

Possible and keep close to PHY all the time.