Four parallel time samples (acquired at 4x the FPGA clk rate) are passed from the ADC to the 4 tap Polyphase Filter Bank. Between the two blocks, a "downshift" at 1/4 of the ADC clock rate (200 MHz if sampling)

This is necessary because of limited BRAM resources on the IBOB the FFT cannot overflow (see FFT documentation for details on why

The resultant signal is 8 bits I, 8 bits Q, representing the

This design is set for a maximum

800 Msps).

The "prog_delay" block allows the signals from pol1 and pol2 of antenna 1 to be

This allows a computer to know when

or

new_acc

This can be done through the "eq_coeff" software

coefficient ("coeff"), and then using "coeff_en" to write the new coefficient into the equalization table. In this design,

a non-periodic order) to avoid favoring certain frequencies.

Of the output 32 bits, 16 represent "whole bits", and 16