Phased Array VLBI Processor for SMA

PHased-array Recording INstrument for Galactic Event-horizon Studies

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VLBI Project PI: Sheperd Doeleman (& many VLBI collaborators at Haystack and elsewhere)

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A phased array processor...
...using existing systems...

- SMA computer controls a DDS providing a 109 MHz phase-reference for locking the LO
- Used to implement fringe stopping, 0°-180° Walsh switching (not normal mode), and phase corrections
- 1024 MHz of IF tapped-off from each antenna
...using existing systems...

- 10 MHz maser reference used to clock all digital hardware
- 1 PPS provided via GPS for VLBI clock syncing
- 100 Hz “heartbeat” used for data alignment
Two 512 MHz sub-bands, 512-1024 MHz (low) and 1024-1536 MHz (high)

Amplifiers and adjustable attenuators provide adjustable analog power levels
...and CASPER electronics

5 iADCs for sampling at 1024 MHz and clocking fabric,

3 iBOBs, for processing time-domain samples and shipping to storage terminal,

and a single BEE2 corner chip for a 7-baseline calibration correlator
System deployment and test

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iBOB delay compensation

BEE2 calibration correlator

Mark5B+ # 1

Mark5B+ # 2

Linux control computer

Analog phase compensation

UPS power conditioning

Analog Pre-Processors
After sampling...

- The 8-bit, demux-by-4 data is delay-corrected to get fringes within the correlator span.
- In practice, geometric delays are all that’s needed (after calibrating constant systematics).
...the data is de-Walshed...

- de-Walshing also occurs at this stage by simply switching the signs of samples
- Walsh states are received from the DDS computer on a ribbon cable attached to the GPIO
- Removes spurious sources of correlation such as the strong cross-talk between iADC inputs
- Greatly improves the sensitivity of the calibration correlator and is required by VLBI
...delays are compensated...

- Vinayak Nagpal’s beamformer design
- Coarse delay, using a 2000-sample deep FIFO for ~8us of delay at 4ns step size
- Accounts for the SMA in Very EXtended

Figure 18: V. Nagpal’s Master’s Thesis
...delays are compensated...

- Fine delay, a barrel-selecting arrangement providing a smaller step size of 1 sample, ~1ns
- and...

Figure 19: V. Nagpal’s Master’s Thesis
...delays are compensated...

- “Superfine” delay, provided by a 10-tap, demux-by-4, FIR interpolating filter provided a step size of 0.1 ns

- Please refer to Vinayak’s thesis for more details

Figure 22: V. Nagpal’s Master’s Thesis
a single tap
• Phase corrections (measured by the calibration correlator) are applied to the 109 MHz reference by the SMA DDS

• Standard SMA fringe-stopping is always occurring
...the data is summed...

- 8-bit, demux-by-4, phased-up samples are multiplied by gain factors
- Used for weighting and inclusion/exclusion of any number of antennas from the sum
- Each iBOB Beamformer sums 4 antennas and sends its sum out over XAUI for the last sum
(well it turns out...

...the XAUI samples need to be aligned)
...and it’s stored for VLBI

- Last iBOB implements a modified Haystack digital back-end
- Data is shipped over VSI for fast storage on a Mark5B+
- (and then the packs are literally shipped to Haystack for correlation)
The calibration loop...

- Uses cross-correlation to extract the necessary delays and phases
- Antenna streams are correlated to one reference
- XA is done on the BEE2 while F and phase-fitting is done in software
...uses 2-bit samples...

- A single ROM per stream per antenna is used to quantize to 2-bits
- Threshold is adjustable and optimal level can be found using 2-bit histograms on BEE2
- Data is further demuxed by 2 and two groups of 4 are sent over XAUI to the calibration correlator
...an XF architecture...

- BEE2 is run on a synchronous clock generated by upstream iBOB\textsuperscript{s} at 128 MHz
- Correlator architecture is demux-by-8 with 16 positive and 16 negative lags
- Currently 7 baselines on one chip
...an XF architecture...

- Multipliers are Xilinx ROM primitives, 4-input LUTs
- Accumulations are typically 16-30s to pull out the source but unexplained offsets are often limiting
a single lag
...and Python software

- Software reads off correlation functions from the BEE2
- Takes an FFT and finds amplitude and phase
- De-wraps phase if necessary
- Fits a straight line to the phase and feeds back y-offset and slope
Possible improvements

• Remove large DC offsets in the correlator that do not go away with Walshing
• Separate the other sideband
• Perform 90°-270° de-Walshing for parallel observations with the SMA
• Find better method to confirm increased SNR
• Use a more sophisticated method for selecting when to apply measured phases
• Automate 2-bit quantizer’s level control
Future

• Migrate to ROACH
• Other architectures (FX, cascaded, etc.)
• Larger bandwidths
• Faster data storage