The Whole Sort of General Mish Mash

Frequently Asked Questions and Trip-ups
About the CASPER Libraries and Toolflow

Henry Chen, CASPER Workshop, August 2008
Number Representation

- Follows Matlab/Simulink *fixed-point* notation

- (Data type)_(bit width)_(binary point)
  - Signed (2’s Complement): Fix
  - Unsigned: UFix

- Ex: **32-bit signed** number, **12 bits after binary point**: Fix_32_12

- Ex: **16-bit unsigned integer**: UFix_16_0
Tools Distinction

MSSGE:
- Matlab / Simulink / System Generator / EDK

Merging vendors
- Mathworks / Mathworks / Xilinx / Xilinx

System Generator is a Xilinx-provided toolbox for Simulink; very small subset of Simulink!

Referred to as “Simulink toolflow”, but beware of vendor domains
Simulink Design Domains

- Simulation vs. Implementation
- Implementation domain is FPGA-mappable
  - Uses Xilinx System Generator primitives
  - Fixed-point numbers (Fix, UFix)
- Simulation domain is NOT FPGA-mappable
  - Uses Simulink components
  - Floating-point numbers (double)
- Xilinx provides *gateway* blocks as interface between domains
  - Data type translation
  - Maps to design top level I/O ports
  - Use “yellow blocks” from bee_xps system library
Sample Periods

- Simulink concept of time
- Determines clock periods on FPGA
  - Can implement multi-rate designs (not supported)
  - Only ratios important
- Customarily set to “1” (1 “second” per cycle)
- Xilinx blocks infer sample period based on input
  - All inputs to Xilinx blocks must be connected
  - Turn on “Sampled Constant” for Xilinx Constants
Sync Pulses

- Latency-matched “vector warning” signal
- Each block responsible for managing sync delay and propagation
Sync Pulses (cont’d)

- Resets datapath
  - Startup
  - Realignment
- If repeating, make sure to cover entire data window or frame

Minimum period = \( LCM(\text{reorder orders}) \cdot \frac{\text{FFT Size}}{\text{Simultaneous Inputs}} \cdot \text{Other modifiers} \)
Sync Pulse Generator

- Good to have manual reset capability
Clock Trimming
Clock Trimming

- Running NGCBUILD ...noclock_xsg_core_config_wrapper (noclock_xsg_core_config) -
  /vol/hitz/vol2/designs/CASPER/projects/henry_devel/noclock/XPS_iBOB_base/system.mhs:273 - Running
  NGCBUILD
  ERROR:MDT - :MDT - NgcBuild failed!  INFO:MDT - Refer to
  /vol/hitz/vol2/designs/CASPER/projects/henry_devel/noclock/XPS_iBOB_base/implementation/noclock_xsg_core_config_wrapper.blc for details.
  noclock_xaui_wrapper (noclock_xaui) -
  /vol/hitz/vol2/designs/CASPER/projects/henry_devel/noclock/XPS_iBOB_base/system.mhs:315 - Running
  NGCBUILD
  noclock_adc_wrapper (noclock_adc) -
  /vol/hitz/vol2/designs/CASPER/projects/henry_devel/noclock/XPS_iBOB_base/system.mhs:368 - Running
  NGCBUILD
  ERROR:MDT - Error while running "gmake -f system.make init_bram"
  No changes to be saved in MSS file
  Saved project XMP file

- Loading design module
  "/vol/hitz/vol2/designs/CASPER/projects/henry_devel/noclock/XPS_iBOB_base/implementation/noclock_xsg_core_config_wrapper/noclock.ngc"...
  ERROR:NgdBuild:76 - File  "/vol/hitz/vol2/designs/CASPER/projects/henry_devel/noclock/XPS_iBOB_base/implementation/noclock_xsg_core_config_wrapper/noclock.ngc" cannot be merged into block
  "noclock_xsg_core_config" (TYPE="noclock") because one or more pins on the block, including pin "clk", were not found in the file. Please make sure that all pins on the instantiated component match pins in the lower-level design block (irrespective of case). If there are bussed pins on this block, make sure that the upper-level and lower-level netlists use the same bus-naming convention.
Pink Blocks vs. Green Blocks

- **astro_library (“pink blocks”)**
  - Not updated anymore
  - Old masking technique; always redraws
  - Verified functionality

- **casper_library (“green blocks”)**
  - Current development
  - New masking technique; remembers state
  - Some translation bugs
  - Unified library
Toolflow Setup

- Install vendor tools and service packs
  - Mathworks: Matlab, Simulink
  - Xilinx: System Generator, EDK, ISE
  - Synplicity: Synplify Pro
  - Mentor Graphics: ModelSim

- Get libraries
  - CASPER SVN [http://casper.berkeley.edu/svn/trunk](http://casper.berkeley.edu/svn/trunk)
  - Anonymous read access
  - Nightly tarballs on CASPER website

Toolflow Setup

- Set environment variables
  - Can use batch file if not admin on system or using multiple versions

- Add libraries to Matlab path
  - Use startup.m with `addpath`, `rmpath` functions
  - Startup script needs to be in matlab.exe’s “Start In” directory
  - Do not use UNC paths for “Start In” directory
Matlab Pickiness

- Avoid UNC paths for working directory
- No spaces in working directory path or model filename
- Don’t start model filename with capital letter
How It All Works

- System Generator generates VHDL/Verilog and synthesizes into black-box netlist
  - Calls CoreGen for more complex blocks
  - Gateways in yellow blocks become ports at top level
- bee_xps packages netlist into EDK core
- bee_xps copies a base system package (skeleton project) and instantiates your design
  - Clocking, processor infrastructure
  - Sources for other cores
- Based on yellow blocks, instantiates and connects interface cores
- Runs EDK on project
- Bitstream/BOF out