BabyBEE
Defining the Silicon Circuit Board

CASPER Workshop

August 4, 2008

Bob Conn
CTO
siXis

- Spin-out of Research Triangle Institute
- Started July 3, 2008
- $5.2M
- MiniBee Alpha product already delivered
- BabyBEE available early 2009
- Derivative of BEE2
BabyBEE

- Started with BEE2 at BWRC
- BabyBEE
  - Smaller
  - Faster
  - Cooler
  - Less expensive
  - Lower operating costs
  - Xilinx V5
- Futures with CPUs, other FPGAs, RF, etc.
<table>
<thead>
<tr>
<th></th>
<th>SICB</th>
<th>MCM*</th>
<th>PCB 2007*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board-to-board interconnect density</td>
<td>1600%</td>
<td>625%</td>
<td>100%</td>
</tr>
<tr>
<td>Layers for interconnect to exit BGA</td>
<td>25%</td>
<td>63%</td>
<td>100%</td>
</tr>
<tr>
<td>Pad pitch</td>
<td>24%</td>
<td>40%</td>
<td>100%</td>
</tr>
<tr>
<td>Trace pitch (width plus space)</td>
<td>16%</td>
<td>32%</td>
<td>100%</td>
</tr>
<tr>
<td>Via diameter (through substrate)</td>
<td>60%</td>
<td>90%</td>
<td>100%</td>
</tr>
<tr>
<td>Microvia diameter (not through substrate)</td>
<td>13%</td>
<td>100%</td>
<td>100%</td>
</tr>
<tr>
<td>Maximum substrate size</td>
<td>10%</td>
<td>20%</td>
<td>100%</td>
</tr>
<tr>
<td>Functionality per unit area</td>
<td>10x</td>
<td>10x</td>
<td>1</td>
</tr>
<tr>
<td>Cost per unit functionality</td>
<td>41%</td>
<td>54%</td>
<td>100%</td>
</tr>
<tr>
<td>Reliability</td>
<td>Better</td>
<td>Worse</td>
<td>Average</td>
</tr>
</tbody>
</table>

*The Information Network, Internal RTI analysis*
MiniBEE

- FR-4 based version of BabyBEE
- Architectural verification
- Early adopter software development platform

5” x 10”
22 layer FR-4
V5LX220
BabyBEE

- FPGA die
- Cooling
- SiCB
- Power
32 FPGAs, 256 Memory Chips

BabyBEE = SiCB technology validating application

High performance reconfigurable computing
Excellent application of the SiCB platform

- Designs are scalable
- FPGAs available as known (mostly) good die today
- Rapidly developing market
- High value placed on low power and small size

2” x 3 ½” x 3 ½”
BabyBEE Architecture

A Typical Small System

Compute Board

Local Bus

Shared Bus (black)

Torus Bus (red)
BabyBEE Advantages

- Lower parasitic capacitances (and inductance)
  - Less need for bypassing
- Vertical interconnect density 12:1
- Horizontal wire density 12:1
- Wires are RC, not LC
  - Termination resistors almost eliminated
- Easier to design
  - FR4 already requires a microwave engineer
- Increased I/O density on FPGAs because of smaller I/O drivers
  - Limited by package constraints today
- I/O buffers can be smaller ➔ 6pF to 3pF
  - New chip designs
- Alignment
  - Approximately 1mil for FR4 to 1 micron for SICB
- Stacking memory – the wiring problem is minimum
Desktop Brick

- 4” x 6” x 8”
- 0.35 TFlops (dp)
- 30 TOps (16 bit)
- 16 FPGAs
- 16 GB memory
- 50Gb/s I/O
- < $100k
The Cube

Just for Fun

37 petaOps (16 bit int)

The Cube
27" x 34" x 28"
8x8x8
< $100M
4096 BabyBEE Boards
16,384 FPGAs
18 TB memory
500kW
360 Tflops (dp)
37 petaOps
#1 Supercomputer
Maximum latency across
The Cube < 20ns
# BabyBEE Products

<table>
<thead>
<tr>
<th></th>
<th>PCB Package</th>
<th>Brick</th>
<th>Cube</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size mm</strong></td>
<td>80 x 100 x 10</td>
<td>100 x 100 x 50</td>
<td>1000x1000x1000</td>
</tr>
<tr>
<td><strong>FPGAs</strong></td>
<td>4</td>
<td>32</td>
<td>16,384</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>4GB</td>
<td>32GB</td>
<td>16 TB</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>150W +12v</td>
<td>1200W +48v</td>
<td>500kW +48v</td>
</tr>
<tr>
<td><strong>GP I/O</strong></td>
<td>560</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td><strong>Serial I/O</strong></td>
<td>0</td>
<td>40-80 channels</td>
<td>more if needed</td>
</tr>
</tbody>
</table>
FX Correlator (ATA350, single IF) in 144 BEE2 modules

- Size is connector limited
- I/O: Expect 5Gb/s per channel ➔ 6 BabyBEE I/O Modules

44 BEE2 modules for PFB & CRB
100 BEE2 modules for XMAC
Single 144 port Infiniband switch

Specs:
N = 350
M = 1024
R_{sample} = 100MHz

Input Bitwidth = 4, 4
Polarization = 2
Dump time = 10ms ~ 30s
Output Bitwidth = 32
## Scaling of the BEE2 architecture

<table>
<thead>
<tr>
<th></th>
<th>ATA 350</th>
<th>SKA 2000</th>
<th>SKA 4400</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Radio Telescope</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total IF bandwidth in GHz</strong></td>
<td>0.4</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td><strong>Antennas</strong></td>
<td>350</td>
<td>2000</td>
<td>4400</td>
</tr>
<tr>
<td><strong>Beam</strong></td>
<td>16</td>
<td>128</td>
<td>512</td>
</tr>
<tr>
<td><strong>Correlator comp. req. (CMac/s)</strong></td>
<td>4.9E+13</td>
<td>8E+15</td>
<td>7.744E+16</td>
</tr>
<tr>
<td><strong>Beamformer comp. req. (CMAC/s)</strong></td>
<td>8.96E+12</td>
<td>2.048E+15</td>
<td>3.60448E+16</td>
</tr>
<tr>
<td><strong>BEE2 cost in $M (1X, 2005)</strong></td>
<td>$ 6.10</td>
<td>$ 1,057.84</td>
<td>$ 11,947.57</td>
</tr>
<tr>
<td><strong>BEE3 cost in $M (5X, 2007)</strong></td>
<td>$ 1.22</td>
<td>$ 211.57</td>
<td>$ 2,389.51</td>
</tr>
<tr>
<td><strong>BEE4 cost in $M (25X, ~2009)</strong></td>
<td>$ 0.24</td>
<td>$ 42.31</td>
<td>$ 477.90</td>
</tr>
<tr>
<td><strong>BEE5 cost in $M (125X, ~2011)</strong></td>
<td>$ 0.05</td>
<td>$ 8.46</td>
<td>$ 95.58</td>
</tr>
</tbody>
</table>

July 21th, 2004

BWRC, UC Berkeley
Core Technology and Intellectual Property

Large-area SICBs attempted and failed 15 years ago
- Reliability an issue > 1”x1”
  - Delamination/cracking occurred under routine thermal cycling
- Inadequate interconnect density
- Known good die issue

BEECo’s technology allows reliable 4”x5” SICBs (min.)
- Higher interconnect density, fewer signal layers
  - High aspect ratio through-silicon-vias technology
- Mechanical re-enforcement (rivets)
- Stress-relieving structures (spongy oxide and service loops)

Eight patents filed, 16 disclosures
BabyBEE vs. MiniBEE

FR4 PCB
MiniBEE

SICB
BabyBEE

0.7 TFlops (dp)
60TOps (16bit)
300 Gb/s I/O
8GB memory
800W