REMOVED 3V3 GENERATION

REMOVED +12V GENERATION  REMOVED -12V GENERATION

REMOVED +1V GENERATION  REMOVED +2V5 GENERATION

REMOVED +12V GENERATION  REMOVED -12V GENERATION

REMOVED 3V3 GENERATION

REMOVED +12V GENERATION  REMOVED -12V GENERATION

REMOVED +1V GENERATION  REMOVED +2V5 GENERATION

REMOVED +12V GENERATION  REMOVED -12V GENERATION

REMOVED 3V3 GENERATION

REMOVED +12V GENERATION  REMOVED -12V GENERATION

REMOVED +1V GENERATION  REMOVED +2V5 GENERATION

REMOVED +12V GENERATION  REMOVED -12V GENERATION

REMOVED 3V3 GENERATION
PCI BUS NOT IMPLEMENTED
It is advised to match the trace length within each path to minimize timing skew.
Clock Rules:

- CLK_CPLD_33 MHz = CLK_SYS_33 MHz
- CLK_SYS_33 MHz = as short as possible
- CLK_UART_11.0592 MHz = as short as possible

Clocks:

- CLK_USB2.0_12 MHz = as short as possible
- CLK_CPLD_50 MHz = as short as possible
- CLK_GETH0_25 MHz = as short as possible
- CLK_PCI1_66/33 MHz = Clk_PCI2_66/33 MHz + 2.5"