IBOB Block Diagram

Xilinx Virtex II Pro
2VP50 FPGA

2x diff. clock

40 pair diff. I/O
(ZDOK)

40 pair diff. I/O
(ZDOK)

40 pair diff. I/O
(MDR)

RS232

10/100 Ethernet

Diff. Clock I/O
(SMA)

Configuration
PROM

36x512k
SRAM

36x512k
SRAM

80x GPIO

10 Gbps I/O
(CX4)

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(CX4)

UC Berkeley SETI Group
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