SNAP Board GOAL:

Take it down a notch
The Smart Network ADC Processor (SNAP) board

NRAO: Joe Greenberg, Rich Lacasse, Bob Treacy
Berkeley: Dave Deboer, Matt Dexter, Aaron Parsons, Dan Werthimer
Cambridge/Berkeley: Jack Hickish, JASPER tool flow “It’s not you, it’s me”

https://casper.berkeley.edu/wiki/DAB-HERALD
THREE SNAPLICATIONS

HERA: need short analog cables to minimize reflections
Digitize at Telescope, Channelize (Fengine), Packetize,
Transmit 10Gbe data over 10km using CWDM

Inexpensive Instrumentation: Kintex 7: $250, $1K, $2K FPGA

Entry Level FPGA/ADC/Synth Board for Student Training
($1.5K with Kintex7 160T FPGA)
WHAT’s on BOARD?

ADC’s: 12 inputs 250 Msps,
6 inputs 500 Msps,
3 inputs at 1 Gsps, 8/10/12 bit
1 ZDOC for external ADC board

Frequency Synthesizer (or external sample clock)

Kintex7 FPGA 160T, 325T, or 410T
2x10Gbe SFP+
1 PPS Sync In, 10 MHz In, External Sample Clock In, Digital I/O, 12 Volt Power In

no processor! (but connector for Raspberry PI)
Single shielded enclosure

12 VDC

DC Filtered Connector

Regulators as req'd

SMA

Coax

PAD

BPF

Sine to Square

Sample Rate Input

10 MHz Input

SMA

Coax

FPGA_SYNTH_CTRL

10 MHz PLL

10 MHz PLL

RF_OUT_A

CTRL

LMX2581 Synthesizer

Clock Select

Clock Buff.

FPGA_ADC_CTRL

1.8V, ~400mA

1.8V, ~400mA

HMC1511 ADC

IN_0

IN_1

IN_2

IN_3

Data

Bit & Frame Clocks

1.8V, ~400mA

HMC1511 ADC

IN_0

IN_1

IN_2

IN_3

Data

Bit & Frame Clocks

HMC1511 ADC

IN_0

IN_1

IN_2

IN_3

Data

Bit & Frame Clocks

100 MHz Clk

156.25 MHz Clk

SERDES

10 GbE

10 GbE Fiber

100Base SFP+ Transceiver

100Base SFP+ Transceiver

10 GbE Fiber

Internal LEDs

Buffers

SPI

Conf Mem

GPO

SPI

GPO

SPI

Raspberry Pi

FPGA Bus

Xilinx Virtex 6 FPGA

SERDES

10 GbE

Note 1: Mount this ADC on the bottom of the board to get short clock runs

Note 2: Keep the layout for the balun and termination similar to existing Berkeley design

Note 3: All components are enclosed in an shielded case. I/O is via shielded connector and the 10 GbE fiber is routed out of the case via “wave guide” beyond cutoff.

Note 4: Clock logic for ADC is functional to 1 Gb/s.
THREE Mounting Systems

RFI Tight Enclosure (COMPAC)

CARD CAGE
  (22 boards in 7U, 176 boards per rack)

Stand Alone Lab Bench
Copper, Optical SFP+ 10Gbe Cables
1-10m, 100m, 1km, 10km, 40 km

DWDM, CWDM, BiDi
Status:

Schematics/BOM Done
Design Review Done
Tool Flow ~Done (JASPER)
PCB Layout Half Done

Board Assembly  Late Summer
Test/Debug   Fall/Winter 2014
Revision 2 ?   (add 2nd Zdoc?, more SFP+?)
CASPER PhD’s in last year

- Andrew Siemion
- Danny Price
- Jack Hickish
- Griffin Foster
- Terry Filiba
- Laura Spitler
- Laura Vertatschisch
- Jayanth Chennamangalam
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South African BBQ Team