ROACH3 Introduction

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Technology: ROACH3

- Designed for MeerKAT
- Suitable for SKA-1 F/X/B engines
- 28nm FPGA technology
- 40 Gbps and 100Gbps Ethernet
FPGA

- Virtex 7 XC7VX690T-2-FFG1927
  - 80 GTH Transceivers (11.3 Gb/s for 2C speed grade)
    - 64 TX/RX pairs used for Mezzanine Sites
    - 1 TX/RX pair for 1 Gigabit Ethernet
    - 15 TX/RX pairs used for CPU/GPIO
Configuration

• **Bootstrap Image (non-volatile memory)**
  • Programmed via JTAG
  • Loaded at power-up
  • Loads 1 GigE receiver and configuration memory controller
  • FPGA image received via 1 GigE and written to configuration memory

• **Configuration Memory**
  • Configuration < 1 second
  • Life cycles > 1 000 000
  • Programmable via JTAG and Ethernet through the FPGA
Mezzanine Sites

- 4 Multi-purpose Mezzanine sites
  - 16 TX & RX Transceivers per site
  - Planned Cards
    - 4 x 40 GbE QSFP+
    - Hybrid Memory Cube
  - Possible Cards
    - 12 x 10 GbE SFP+
    - 1 x 100 GbE CFP2
    - JESD204B Optical Interface
Mezzanine Sites

- **400 pin Meg-Array connector (FCI 84740-202LF)**

| A | B | C | D | E | F | G | H | J | K | L | M | N | P | Q | R | S | T | U | V | W | X | Y | Z | AA | AB | AC | AD | AE | AF | AG | AH | AJ | AK | AL | AM | AN | AP | AQ | AR |
| 5V | 12V | VCC (AEJ) | CK1i | CK1o | Vssn | Vcc | Hn | Vccm | SCL | SDA | AD0-3 | Tm | Fn_E | JTAG |

- 16 RX GTH pairs to green blocks
- 16 TX GTH pairs to yellow blocks
- Remaining grey blocks optional
- 10 x 12V (60W), 20 x 5V (50W)
- VCC (ADJ) optional, Voltage request via 1W (EEPROM), Vssn+/ for voltage sag compensation, Vccm for voltage monitoring. SD allows mezzanine card to request VCC shutdown. *Not connected in this design.*
- CK1i: Differential clock sourced from motherboard
- CK1o: Differential clock sourced from mezzanine
- 1-wire EEPROM interface (1-W) used to identify card to motherboard.
- Hn: Presence detect (adds mezzanine to JTAG chain)
- SCL, SDA: I2C bus
- AD0-3: Address
- Tm: Temperature monitor
- Fn_E: Fault not-Enable
- JTAG
QSFP+ Mezzanine Card

- 4 ports per Mezzanine
- 4 x 10.3125 GHz Lanes per Port
- 16 TX/RX Transceivers used

Specified to work with 7m passive loopback cables at full speed on all 4 ports.
• Hybrid Memory Cube Mezzanine
  • 2 or 4 Link Cubes
  • 16 TX/RX Transceivers running at 10 Gb/s
  • 128 Gb/s Read/Write at 80% bandwidth utilization
  • 2 and 4 GB modules
• Separate sampling and processing boards
• Move towards JESD204B serial data link standard
• Interesting part from TI
  • ADC12J4000 - 12-Bit, 4.0 GSPS
• Volunteers to develop ADC / JESD204B interface Mezzanine card?
CPU/GPIO Mezzanine

- General purpose Mezzanine site
- Same connector as normal Mezzanine sites but male / female swapped to create unique card
- 15 RX & TX GTH pairs
- LVDS pairs to remainder (grey blocks)
- No plans to develop CPU Mezzanine by SKA-SA
Power

- Power scheme
  - Power / Temperature Monitoring and Automatic safety shutdown for out of range conditions
  - Soft power-up option – Simulates power button press when mains power is applied and shutdown functionality still works
  - Hard power-up option – Board forced on when mains power is applied, all other power functionality overridden.
- Fan Speed control
- JTAG interface through USB using FTDI
Power

- External power supplied via a 1U ATX supply
  - Xeal Power TC-1U20FX2
  - 200W
- Power
  - FPGA ~ 70W
  - Hybrid Memory Cubes ~ 70W
  - Mezzanine sites rated to 60W @ 12V & 50W @ 5V
• **Board Support Package**
  • Ethernet Cores (1 GigE & 40 GbE)
  • Configuration Memory Controller
  • Monitoring via 1 GigE
    • I2C Monitoring of Temperature, Voltage and Current. Demonstrate safety shutdown.
    • I2C Fan Monitoring and Control
• High technology electronics company in Cape Town in operation for 27 years.
• Designs and manufactures high spec digital wideband radio receivers used for monitoring and direction finding of radio transmissions.
• Also works with select partners on Radar, Sonar and medical products.
• Strong culture of quality in the organisation. Low staff turnover.
• Prioritises giving superb service to a few select clients over growing their customer base.
• Peralex and SKA engineers have worked well together on the digitiser housing.
Schedule

• Currently working on delta concept design review
• Preliminary design review – Late 2014
• 2 Prototype ROACH3 LRUs – Early 2015
• Critical design review – Early 2015
• First production unit – Middle 2015
• “ROACH3” is a departure from the ROACH format
• Need for new acronym?
Acronyms!

- **TERMITE**
  - TE – Terabit (a bit of a stretch…)
  - R – Reconfigurable
  - M – Multi
  - IT – Interface
  - E – Electronics
• TINAR
  T – This
  I – Is
  N – Not
  A – A
  R – ROACH
• SKARAB

SKA – Square Kilometer Array

R – Reconfigurable

A – Application

B – Board
Acronyms!

- NAAI Masjien
  N – Novel / Networking
  A – Architecture for
  A – Astronomy
  I – Instrumentation
Thank you

Questions and comments?